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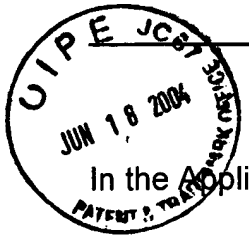


**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
(Case No. 219.003-US)

In the Application of: **Yamada** ) Group Art Unit: **2829**
)
Serial No: **09/865,528** ) Before Examiner: **V. Nguyen**
)
Filed: **May 29, 2001** )
)
Title: **Semiconductor Device Test Method and Semiconductor Device Tester** )
)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 15, 2004
Date
Michiko Sites
(person signing this certificate)
Michiko Sites
Signature

## SUBMISSION OF ENGLISH TRANSLATIONS

Dear Sir:

Attached hereto is an English translation of each of the following Japanese patent applications: JP H9-61142 and JP H8-5528, which were submitted in an Information Disclosure Statement dated March 17, 2004.

Respectfully submitted,

Date: June 15, 2004

Neil A. Steinberg
Reg. No. 34,735
650-968-8079